NV

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,362	09/25/2003	Nikki L. Edleman	FIS920030207US1	2361

29154 7590 01/12/2005

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,362	EDLEMAN ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/03, 9/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because of minor informalities. The examiner notes that in Figure 2A the label 20 should be next to the lead line pointing to the polysilicon layer. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The examiner believes the description of Figures 1, 2A-2F and 4 is considered Prior Art by Applicants. The examiner reminds Applicants of their duty to disclose information material to patentability according to 37 CFR 1.56. Figures 1, 2A-2F and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The examiner refers Applicants to MPEP 2129 [R-2] regarding admissions by applicant constituting prior art. "A statement by an applicant during prosecution identifying the work of another as "prior art" is an admission that that work is available as prior art against the claims, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories of 35 U.S.C. 102. Riverwood Int 'l Corp. v. R.A. Jones & Co., 324 F.3d 1346, 1354, 66 USPQ2d 1331, 1337 (Fed Cir. 2003). However, even if labeled as "prior art," the work of the same inventive entity may not be considered prior art against the claims unless it falls under one of the statutory categories. Id.; see also Reading & Bates Construction Co. v. Baker Energy Resources Corp., 748 F.2d 645, 650, 223 USPQ 1168, 1172 (Fed. Cir. 1984)

("[W]here the inventor continues to improve upon his own work product, his foundational work product should not, without a statutory basis, be treated as prior art solely because he admits knowledge of his own work. It is common sense that an inventor, regardless of an admission, has knowledge of his own work.").

Consequently, the examiner must determine whether the subject matter identified as "prior art" is applicant's own work, or the work of another. In the absence of another credible explanation, examiners should treat such subject matter as the work of another." (Emphasis added.)

Applicant has a duty to disclose that art which he regards as his own as per MPEP 2129. Figures 1, 2A-2F and 4 will be held as "prior art".

Specification

The disclosure is objected to because of the following informalities: in paragraph [0029] the examiner suggests representing the chemical compounds with subscripts. For example chlorine should be represented as "Cl_2" rather than "Cl2".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites a halogen based chemistry that comprises 5% to 95% chlorine-type reactants and less than 5% fluorine-type reactant. The examiner notes that chlorine and fluorine are considered halogens which are a type of reactants. It is unclear what is meant by "chlorine-type" reactant. Is this a reactant that acts as chlorine does in a reaction (i.e. halogen)? Or does this require a reactant that contains chlorine. Similarly, it is unclear what is meant by "fluorine-type" reactant. Is this a reactant that acts as fluorine does in a reaction (i.e. any halogen)? Or does this require a reactant that contains fluorine. The examiner requests clarification. For purposes of examination, the examiner has considered "chlorine-type" and "fluorine-type" reactants as reactants that contain at least one chlorine and at least one fluorine atom, respectively. Claims 23-26 are rejected for being dependent on claim 22.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajeevakumar (U.S. Patent No. 5,283,453) in view of Diodato et al. (U.S. Patent No. 2002/0079522).

In re claim 1, Rajeevakumar discloses the method of manufacturing a deep trench capacitor structure, said method comprising; forming a trench in a substrate;

forming titanium nitride columns (26) in said trench;

dry etching said titanium nitride columns using halogen-based gas phase chemistry to remove an upper portion of said titanium nitride columns (see Figure 6, and column 3, lines 30-40 and column 4, lines 14-16); and

filling a space between said titanium nitride columns and said upper portion of said trench with polysilicon material (28).

Rajeevakumar does not disclose the method wherein the dry etching the titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting surrounding materials.

Diodato et al. disclose a method of dry etching said titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting surrounding materials (see [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dry etch said titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper

portion of said titanium nitride columns without affecting surrounding materials of Diodato et al., because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because as Diodato et al. teach the method of removing the titanium nitride ensures electrical isolation from subsequently formed connections (see Diodato et al. [0047]).

In re claim 2, the combined Rajeevakumar and Diodato et al. disclose the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (Rajeevakumar, 28).

In re claim 3, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen-based chemistry is substantially fluorine free (see Rajeevakumar column 4, lines 14-16).

In re claim 4, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen based chemistry has less than 5% fluorine (see Rajeevakumar column 4, lines 14-16).

In re claim 5, the combined Rajeevakumar and Diodato et al. disclose method wherein said etching process comprises using a decoupled power source that is substantially free of bias (see Diodato et al. [0049]).

In re claim 6, the combined Rajeevakumar and Diodato et al. disclose the method wherein said etching process comprises using a decoupled power source with a bias power of less than 100 W (see Diodato et al. [0049]).

In re claim 7, the combined Rajeevakumar and Diodato et al. disclose the method, wherein said etching process is substantially ion-free (see Diodato et al.

[0049]). The examiner notes that Applicants teach a process which is bias free is ion free. Thus, the method of Diodato et al., which has no bias, is ion free.

In re claim 8, Rajeevakumar discloses the method of manufacturing a trench capacitor structure, said method comprising:

forming titanium nitride (26) columns in a trench;

etching said titanium nitride columns using halogen-based chemistry to remove an upper portion of said titanium nitride (see Figure 6, and column 3, lines 30-40 and column 4, lines 14-16); and

filling a space between said titanium nitride columns and said upper portion of said trench with polysilicon material (28).

Rajeevakumar does not disclose the method wherein etching the titanium nitride columns using halogen-based gas phase chemistry that is substantially ion free to remove an upper portion of said titanium nitride columns.

Diodato et al. disclose a method of dry etching the titanium nitride columns using halogen-based gas phase chemistry that is substantially ion free to remove an upper portion of said titanium nitride columns (see [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dry etch said titanium nitride columns using halogen-based gas phase chemistry that is substantially ion-free to remove an upper portion of said titanium nitride columns of Diodato et al., because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because

as Diodato et al. teach the method of removing the titanium nitride ensures electrical isolation from subsequently formed connections (see Diodato et al. [0047]).

The examiner notes that Applicants teach a process which is bias free is ion free. Thus, the method of Diodato et al., which has no bias, is ion free.

In re claim 9, the combined Rajeevakumar and Diodato et al. disclose the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (Rajeevakumar, 28).

In re claim 10, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen-based chemistry is substantially fluorine free (see Rajeevakumar column 4, lines 14-16).

In re claim 11, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen based chemistry has less than 5% fluorine (see Rajeevakumar column 4, lines 14-16).

In re claim 12, the combined Rajeevakumar and Diodato et al. disclose method wherein said etching process comprises using a decoupled power source that is substantially free of bias (see Diodato et al. [0049]).

In re claim 13, the combined Rajeevakumar and Diodato et al. disclose the method wherein said etching process comprises using a decoupled power source with a bias power of less than 100 W (see Diodato et al. [0049]).

In re claim 14, the combined Rajeevakumar and Diodato et al. disclose the method, wherein said etching process is substantially isotropic (see Diodato et al. [0049]).

In re claim 15, Rajeevakumar discloses a method of manufacturing a deep trench capacitor structure, said method comprising:

forming a trench (14) in a substrate (10);

lining said trench with a polysilicon liner (20);

forming titanium nitride columns (26) along said polysilicon liner;

dry etching said titanium nitride columns using halogen based chemistry to remove an upper portion of said titanium nitride columns, wherein said etching process attacks only in the uppermost portion of said titanium nitride columns such that, after said etching process is completed, the remaining lower portions of said titanium nitride columns are substantially unaffected by said etching process (see Figure 6, and column 3, lines 30-40 and column 4, lines 14-16) ; and

filling a space between said titanium nitride columns and said upper portion of said trench with additional polysilicon material (28).

Rajeevakumar does not disclose the method wherein the etching said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns.

Diodato et al. disclose a method of dry etching wherein the etching said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting the layer below (see [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to etch said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting the layer below, because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because as Diodato et al. teach the method of removing the titanium nitride ensures electrical isolation from subsequently formed connections (see Diodato et al. [0047]).

In re claim 16, the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (28).

In re claim 17, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen-based chemistry is substantially fluorine free (see Rajeevakumar column 4, lines 14-16).

In re claim 18, the combined Rajeevakumar and Diodato et al. disclose the method wherein said halogen based chemistry has less than 5% fluorine (see Rajeevakumar column 4, lines 14-16).

In re claim 19, the combined Rajeevakumar and Diodato et al. disclose method wherein said etching process comprises using a decoupled power source that is substantially free of bias (see Diodato et al. [0049]).

In re claim 20, the combined Rajeevakumar and Diodato et al. disclose the method wherein said etching process comprises using a decoupled power source with a bias power of less than 100 W (see Diodato et al. [0049]).

In re claim 21, the combined Rajeevakumar and Diodato et al. disclose the method, wherein said etching process is ion-free (see Diodato et al. [0049]). The examiner notes that Applicants teach a process which is bias free is ion free. Thus, the method of Diodato et al., which has no bias, is ion free.

In re claim 22, Rajeevakumar discloses a method of manufacturing a deep trench capacitor structure, said method comprising:

forming a trench (14) in a substrate (10);

lining said trench with a polysilicon liner (20);

forming titanium nitride columns (26) along said polysilicon liner;

dry etching said titanium nitride using halogen based chemistry that columns using halogen based chemistry to remove an upper portion of said titanium nitride columns wherein said halogen-based chemistry comprises 5%-95% chlorine-type reactants and less than 5% fluorine-type reactants (see column 4, lines 14-16); and

filling a space between said titanium nitride columns and said upper portion of said trench with additional polysilicon material (28).

Rajeevakumar does not disclose the method wherein the dry etching the titanium nitride based chemistry that columns using halogen based chemistry that is substantially ion free to remove an upper portion of said titanium nitride columns without affecting the layer below.

Diodato et al. disclose the method wherein the dry etching the titanium nitride based chemistry that columns using halogen based chemistry that is substantially ion free to remove an upper portion of said titanium nitride columns without affecting the layer below (see Diodato et al. [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dry etch the titanium nitride based chemistry that columns using halogen based chemistry that is substantially ion free to remove an upper portion of said titanium nitride columns without affecting the layer below, because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because as Diodato et al. teach the method of removing the titanium nitride ensures electrical isolation from subsequently formed connections (see Diodato et al. [0047]).

The examiner notes that Applicants teach a process which is bias free is ion free. Thus, the method of Diodato et al., which has no bias, is ion free.

In re claim 23, the combined Rajeevakumar and Diodato et al. disclose the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (Rajeevakumar 28).

In re claim 24, the combined Rajeevakumar and Diodato et al. disclose the method wherein said etching process comprises using a decoupled power source that is substantially free of bias (Diodato et al. [0049]).

In re claim 25, the combined Rajeevakumar and Diodato et al. disclose the method wherein said etching process comprises using a decoupled power source with a bias power of less than 100 W (Diodato et al. [0049]).

In re claim 26, the combined Rajeevakumar and Diodato et al. disclose the method, wherein said etching process is substantially isotropic (Diodato et al. [0049]).

Claims 1-4 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajeevakumar (U.S. Patent No. 5,283,453) in view of Alers et al. (U.S. Patent No. 6,750,495)

Rajeevakumar discloses the method of manufacturing a deep trench capacitor structure, said method comprising; forming a trench in a substrate;

forming titanium nitride columns (26) in said trench;

dry etching said titanium nitride columns using halogen-based gas phase chemistry to remove an upper portion of said titanium nitride columns (see Figure 6, and column 3, lines 30-40 and column 4, lines 14-16); and

filling a space between said titanium nitride columns and said upper portion of said trench with polysilicon material (28).

Rajeevakumar does not disclose the method wherein the dry etching the titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting surrounding materials.

Alers et al. disclose a method of dry etching said titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting surrounding materials (see column 3, lines 30-55 and column 4, lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dry etch said titanium nitride columns using halogen-based gas phase chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting surrounding materials of Alers et al., because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because as Alers et al. teach the method of removing the titanium nitride ensures prevention of electrical short due to planarization step fo CMP (see Alers et al., column 5, lines 35-45).

In re claim 2, Rajeevakumar discloses the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (28).

In re claim 3, the combined Rajeevakumar and Alers et al. disclose the method wherein said halogen-based chemistry is substantially fluorine free (see Alers et al. column 4, lines 30-35).

In re claim 4, the combined Rajeevakumar and Alers et al. disclose the method wherein said halogen based chemistry has less than 5% fluorine (see Alers et al. column 4, lines 30-35).

In re claim 15, Rajeevakumar discloses a method of manufacturing a deep trench capacitor structure, said method comprising:

forming a trench (14) in a substrate (10);

lining said trench with a polysilicon liner (20);

forming titanium nitride columns (26) along said polysilicon liner;

dry etching said titanium nitride columns using halogen based chemistry to remove an upper portion of said titanium nitride columns, wherein said etching process attacks only in the uppermost portion of said titanium nitride columns such that, after said etching process is completed, the remaining lower portions of said titanium nitride columns are substantially unaffected by said etching process (see Figure 6, and column 3, lines 30-40 and column 4, lines 14-16) ; and

filling a space between said titanium nitride columns and said upper portion of said trench with additional polysilicon material (28).

Rajeevakumar does not disclose the method wherein the etching said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns.

Alers et al. disclose a method of dry etching wherein the etching said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting the layer below (see column 3, lines 30-55 and column 4, lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to etch said titanium nitride columns using halogen based chemistry that is substantially isotropic to remove an upper portion of said titanium nitride columns without affecting the layer below of Alers et al., because as Rajeevakumar teaches any known etching technique could be used to etch the titanium nitride (see column 3, line 65 through column 4, line 17), and because as Alers et al. teach the method of removing the titanium nitride ensures prevention of electrical short due to planarization step of CMP (see Alers et al., column 5, lines 35-45).

In re claim 16, Rajeevakumar discloses the method wherein said process of filling said space simultaneously forms a polysilicon plug and polysilicon cap (28).

In re claim 17, the combined Rajeevakumar and Alers et al. disclose the method wherein said halogen-based chemistry is substantially fluorine free (see Alers et al. column 4, lines 30-35).

In re claim 18, the combined Rajeevakumar and Alers et al. disclose the method wherein said halogen based chemistry has less than 5% fluorine (see Alers et al. column 4, lines 30-35).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk